REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. Claims 1 and 10 are amended, claims 11-12 are added and claims 1-12 are pending in the application.

Figure 2 has been amended to ensure consistency with the specification.

The indication of informalities in claim 10 is appreciated. Claim 10 has been corrected as suggested by the Examiner.

Claim 3 stands rejected under 35 USC §112, second paragraph. This rejection is respectfully traversed. The Examiner asserts that the limitation "includes second converting the network data" is indefinite because it cannot be determined whether it is a second instance of the previous claim limitation "converting the test data" or a completely new claim limitation. However, the claim language clearly demonstrates that the "second converting" of claim 3 is distinct from the "converting" of claim 1: the "converting" of claim 1 specifies "converting the test data into analog-based signals" but does not specify any operation on the network data; rather, claim 1 specifies that the "performing" performs prescribed test operations on the network data. Further, claim 3 specifies that the "second converting" is part of the step of "performing prescribed test operations" claim 1, not the "converting" of claim 1.

Finally, claim 3 specifies that "the step of performing prescribed test operations includes second converting the network data ... into the test data."

Hence, the only reasonable interpretation in view of the foregoing is that the claimed "second converting the network data, having a first data rate, into the test data" of claim 3 is a

new claim limitation that is distinct from the "converting the test data into analog-based signals" of claim 1. Hence, the rejection under 35 USC §112, second paragraph should be withdrawn.

Claims 1-3 and 5-9 stand rejected under 35 USC §102(e) in view of US Patent Publication US 2002/0146043 by McRobert et al. This rejection is respectfully traversed.

Each of the independent claims 1 and 10 are directed to an integrated test device. Claim 1 specifies a method in an integrated test device, and claim 7 specifies the integrated network test device. The specification defines at page 3, lines 24-25 an integrated device as a single chip device. Hence, claim 1 requires that the method be implemented using a single chip, and claim 7 requires that the single chip device include the claimed network logic, first test logic, and second test logic.

Further, the limitation of an integrated test device cannot be disregarded, especially since method claim 1 explicitly specifies that the claimed steps are performed by components implemented on the integrated test device (e.g., network logic, first test logic, and second test logic).

Hence, each of the independent claims 1 and 7 specifies an integrated test device, where network logic performs prescribed network device operations and outputs network data based on a media independent interface based protocol; the first test logic on the integrated test device performs prescribed test operations on the network data and outputs test data based on the MII-based protocol. The second test logic converts the test data into analog-based signals for transmission on a prescribed network medium.

Hence, use of the first and second test logic on the integrated test device eliminates the

necessity of commercial physical layer transceivers having fixed clock speeds. These and other features are not disclosed in the applied prior art.

The Examiner asserts in paragraph 6 of the Official Action that McRobert et al. discloses in paragraph 22 a method that includes performing, using network logic on the integrated test device, first network operations on received data based on paragraph 19. However, paragraph 19 describes Figure 1, which discloses a network 5 having a network switch 10, a repeater 12, a second repeater 14, and a multiple port physical layer transceiver 16. (See lines 5-8 of paragraph 19).

In contrast, paragraph 22 of McRobert et al. describes Figure 2, which discloses a PHY transceiver 16, and repeaters 12 and 14. McRobert merely specifies that "the repeaters 12 and 14, as well as the PHY 16, may be integrated on a single chip" (see paragraph 22, lines 10-13).

However, McRobert et al. provides no disclosure whatsoever that the switch 10 is implemented on a single chip, as asserted by the Examiner. Rather, Figure 1 discloses a network 5, and not a single chip. Moreover, the reference to paragraph 3 is pertinent in that repeaters are used to restore timing and amplitude degradation throughout a local area network that provides a connection among a number of independent computing stations within a small areas such as a single building or a group of adjacent buildings.

Hence, McRobert et al. provides no disclosure that the switch 10 would be implemented within the same chip as the repeater 12 the repeater 14, and the physical layer transceiver 16. Moreover, any such assertion is inconsistent with the description in paragraph 3.

Hence, McRobert does not disclose an integrated test device that includes network logic

configured for performing prescribed network device operations and outputting network data based on a media independent interface based protocol, in combination with first test logic configured for outputting test data based on the MII based protocol, and second logic configured for converting the test data from the first test logic into analog-based signals, as claimed.

For these and other reasons, the rejection of independent claims 1 and 10 should be withdrawn.

The rejection of claim 2 is further traversed. As described above, McRobert et al. merely describes in paragraph 22 that the repeaters 12 and 14, and the transceiver 16 may be integrated on a single chip, however there is no disclosure that the network switch 10 also would be part of the single chip, as claimed. Hence, this rejection should be withdrawn.

The rejection of claim 3 is respectfully traversed. The reliance of paragraph 24 is misplaced, especially since paragraph 24 merely describes that the first data rate path 56 converts network data between MII format and 10Mb/s Manchester-encoded signals for transmission and reception on a 10 Mb/s medium, and that the second data rate path 58 converts network data between MII format and a selected 100Mb/s signal format, such as MLT-3 encoded signals. There is no disclosure of converting between 10Mb/s and 100 Mb/s data rates, as asserted.

In fact, paragraph 25 of McRobert et al. explicitly specifies that:

> [t]he multiplexer circuit 60 routes the output of the data path 56 or 58 through a selected media independent interface 22, 24, etc., via the appropriate data bus 48, based on whichever one of the repeater interface 22, 24, etc. is data rate compatible with link partner 50.
>
> (Paragraph 25, lines 3-8).

Hence, paragraph 25 explicitly specifies that the same data rate is maintained. Further, McRobert describes that the network 5 includes two distinct data rate domains, namely the 10Mb/s domain and the 100 Mb/s domain (see paragraph 20). However, there is no disclosure that data is converted and passed across the domains. For these and other reasons, the rejection of claim 3 should be withdrawn.

Claims 4 and 10 stand rejected under 35 USC §103 in view of McRobert et al. and US Patent No. 5, 657,317 to Mahany et al. As shown in the Statement of Common Ownership on page 11 of this paper, McRobert et al. is not available as a reference under 103(c). Hence, this rejection should be withdrawn.

STATEMENT OF COMMON OWNERSHIP

At the time the invention claimed in the subject application was made, the subject application 09/691,913 and US Patent Publication US2002/0146043 by McRobert et al. were owned by, or subject to an obligation of assignment to, the same entity (Advanced Micro Devices, Inc. of Sunnyvale, California).

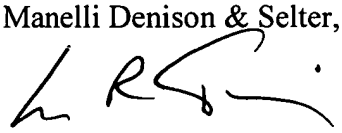
CONCLUSION

In view of the above, it is believed this application is and condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-384, and please credit any excess fees to such deposit account.

Respectfully submitted,

Manelli Denison & Selter, PLLC



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Date: September 2, 2004

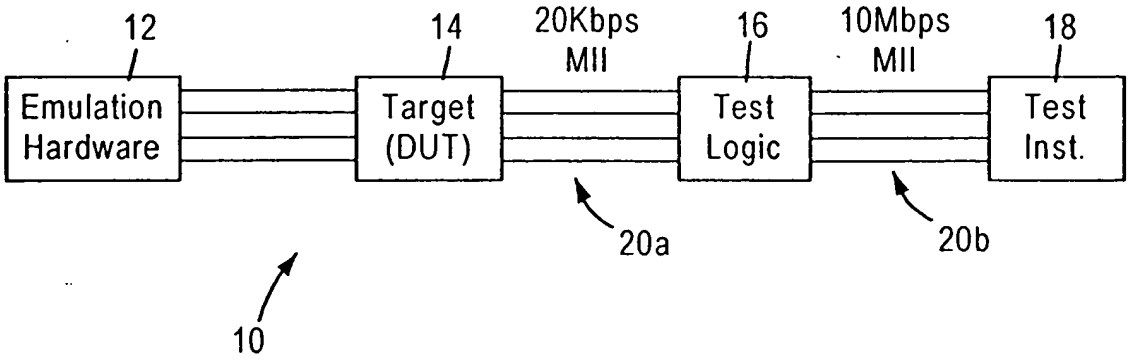

FIG. 1
(PRIOR ART)

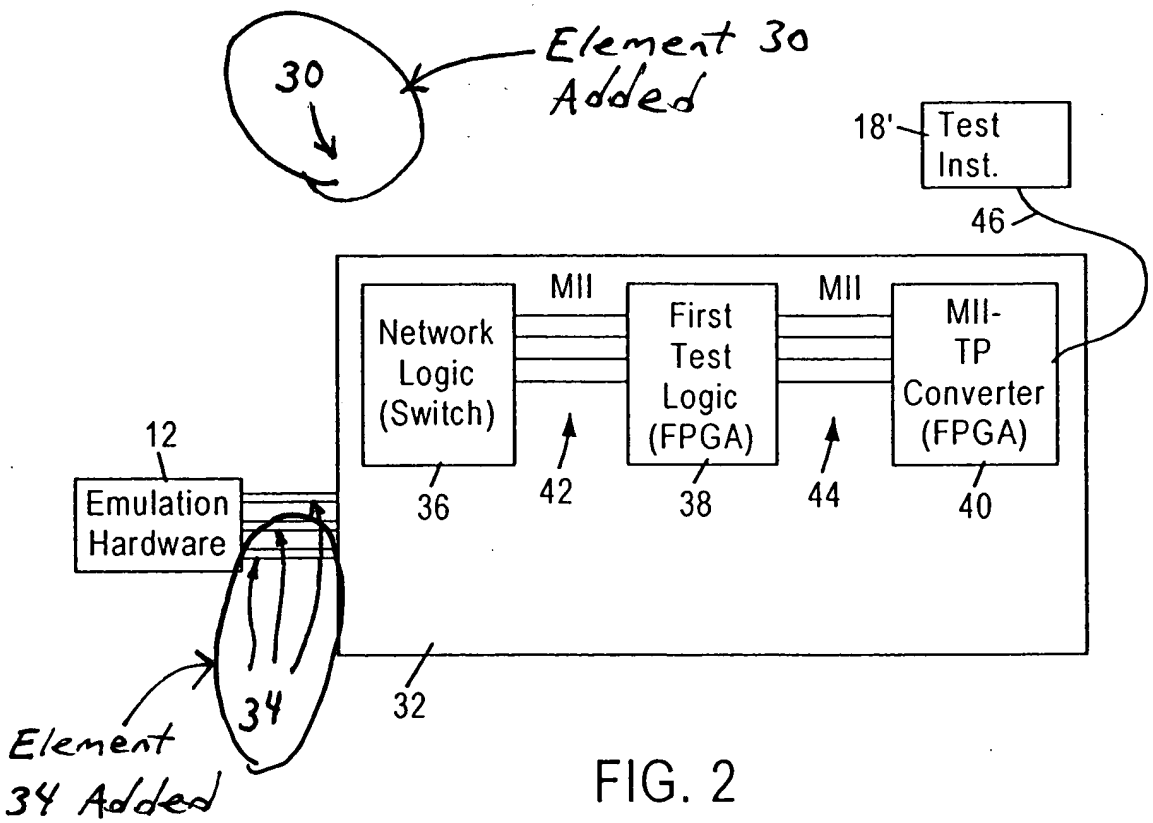

FIG. 2